

FIG. 1

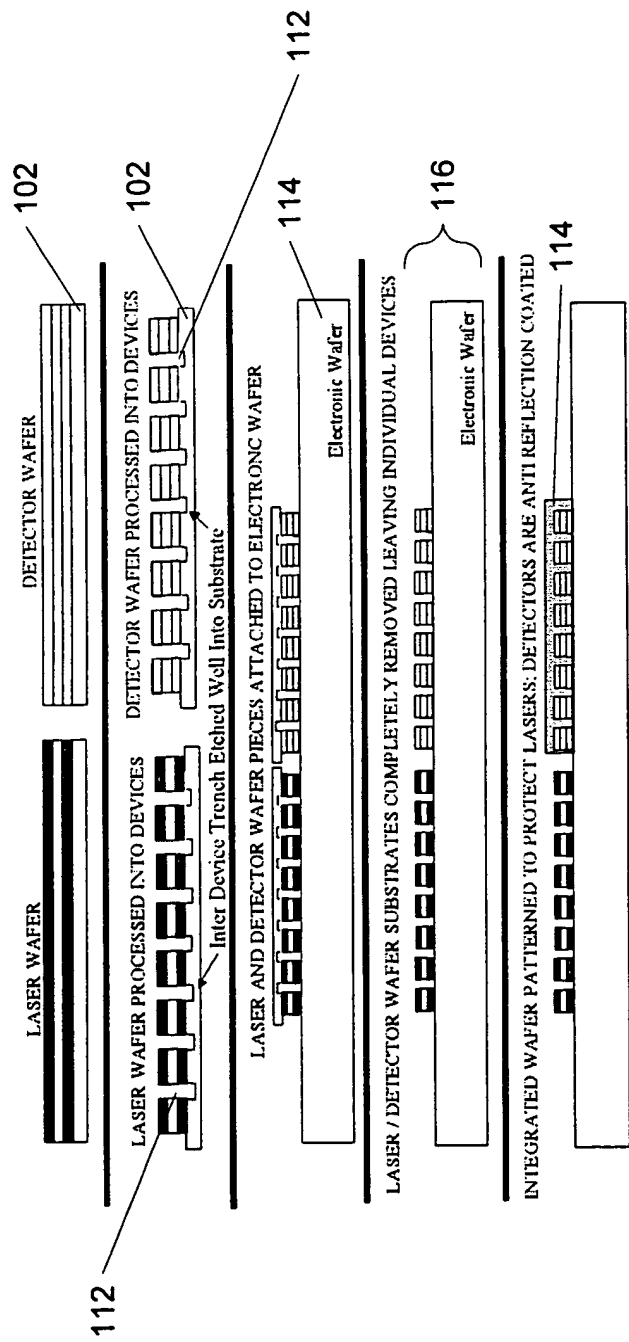


FIG. 2

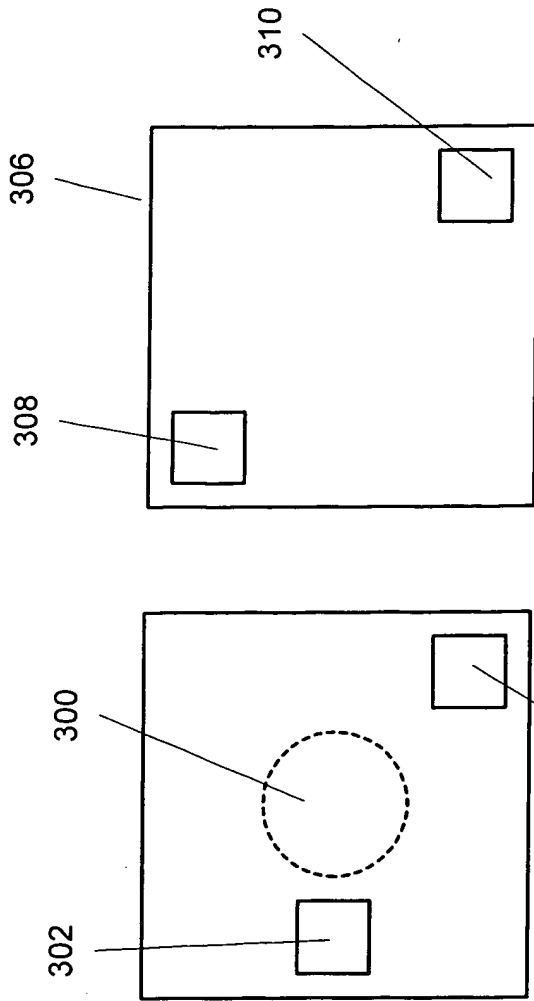


FIG. 3

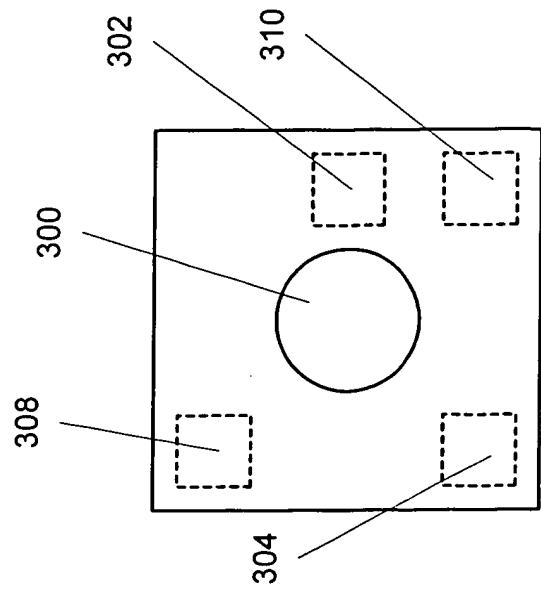


FIG. 4

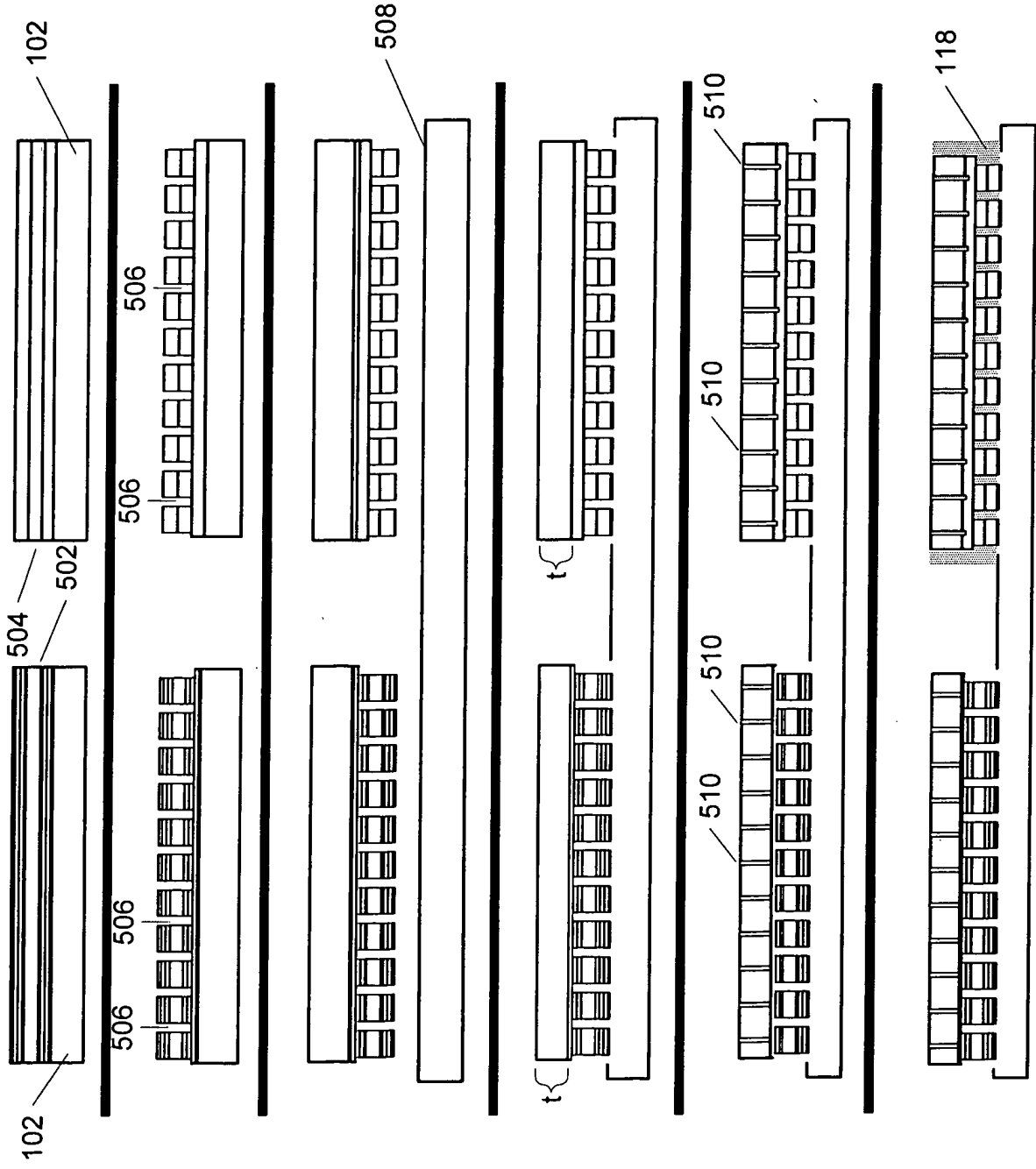


FIG. 5

FIG. 6

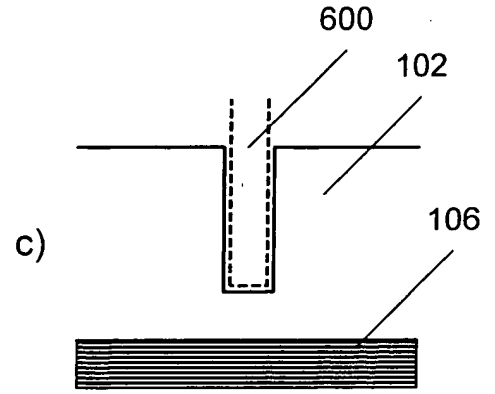
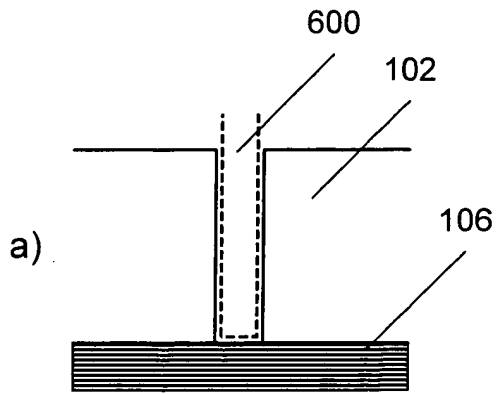
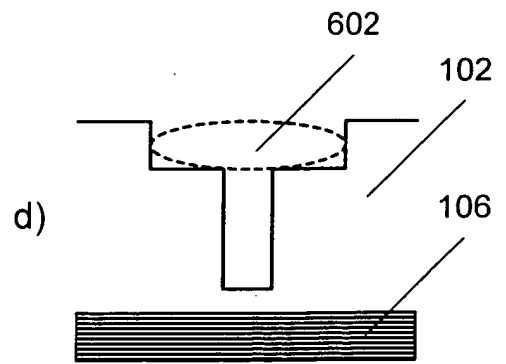
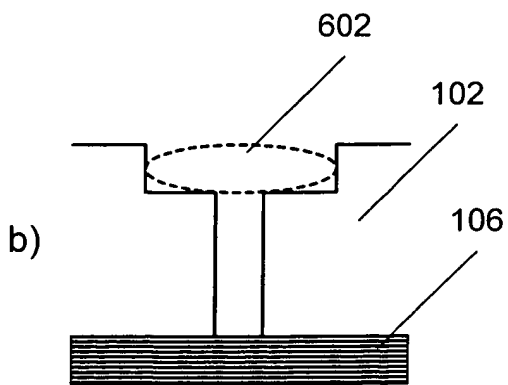


FIG. 6



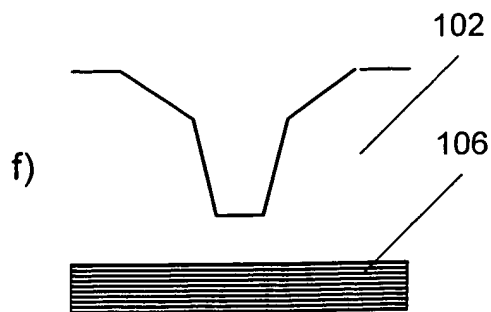
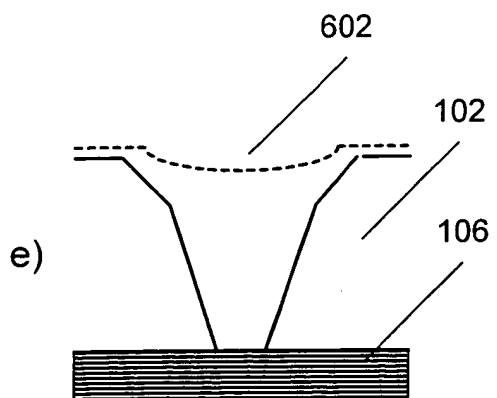
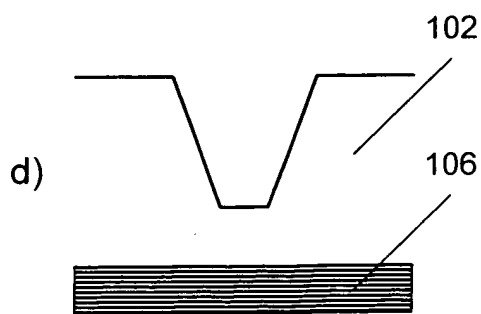
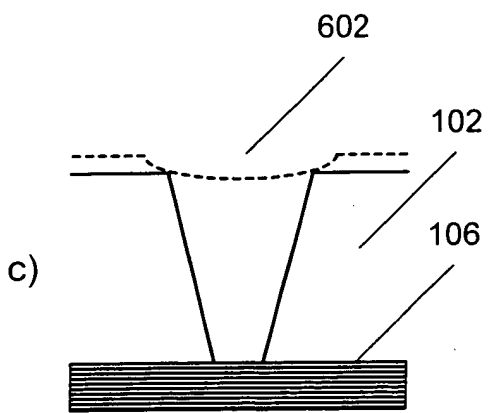
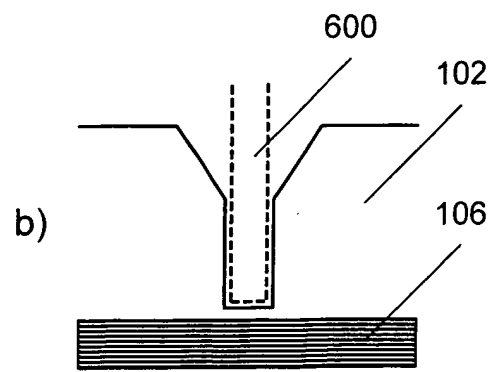
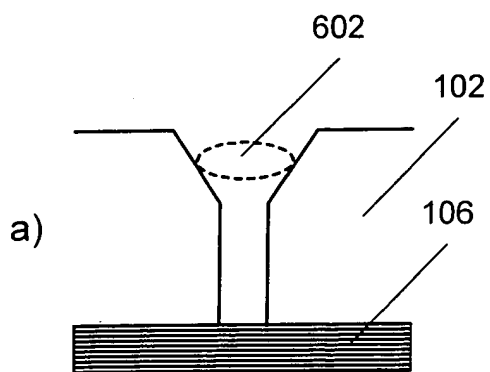


FIG. 7

FIG. 8

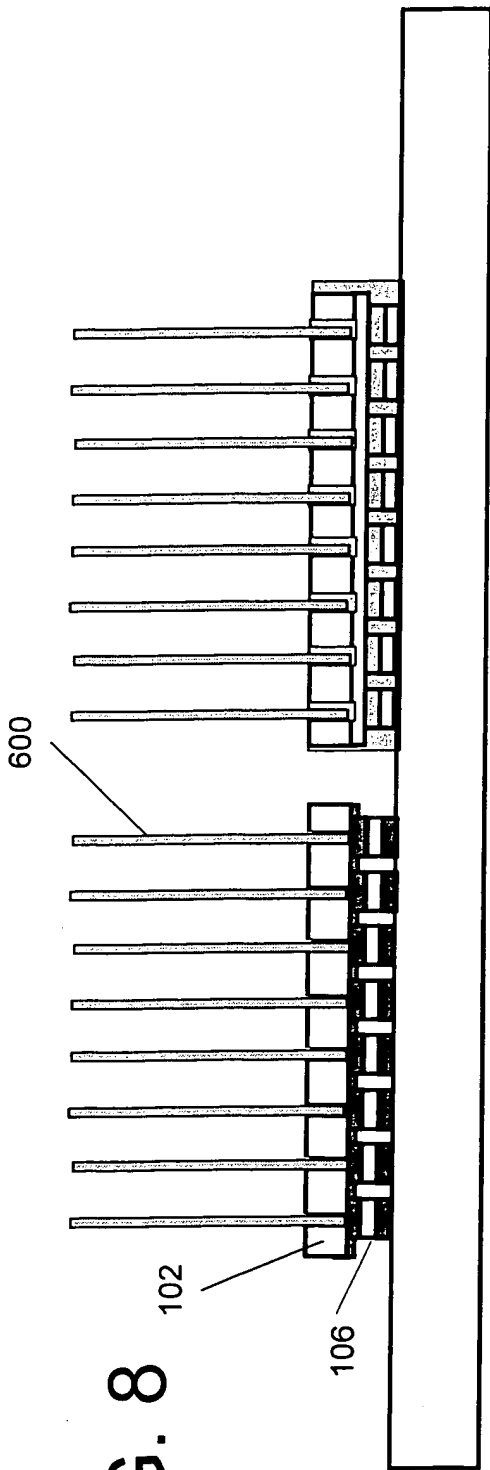
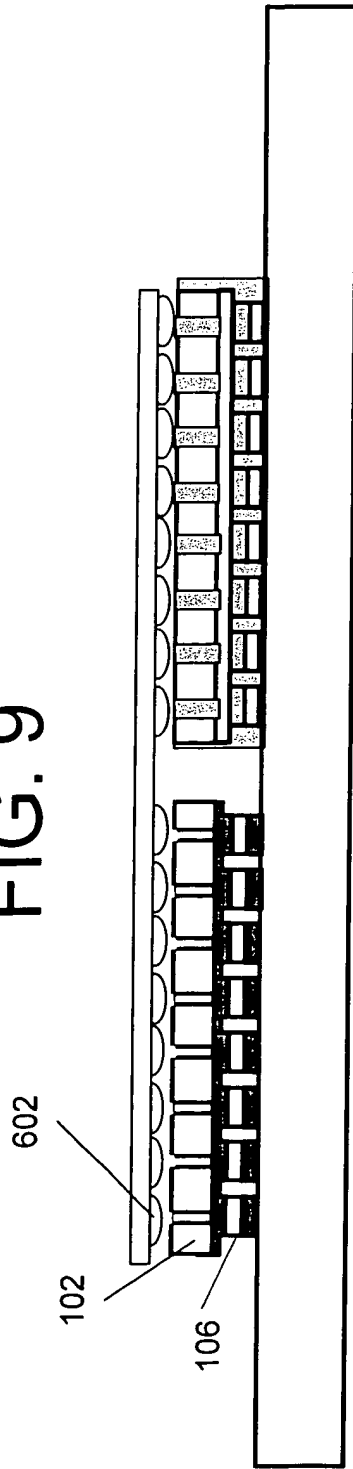
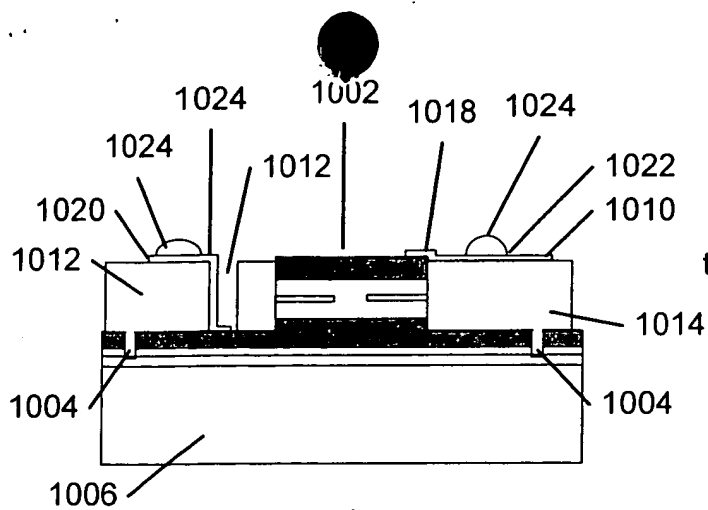
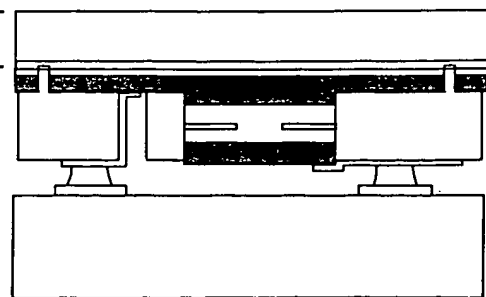


FIG. 9

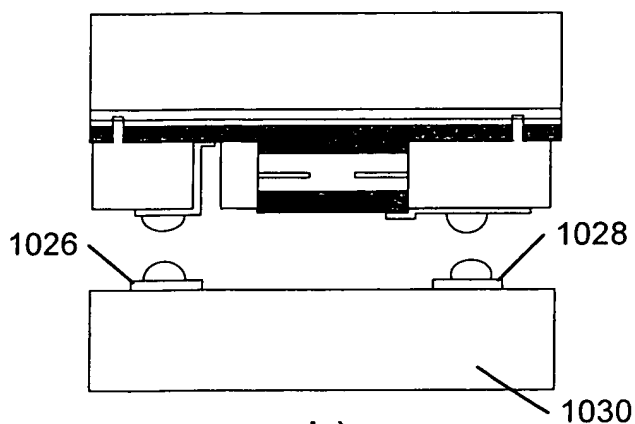




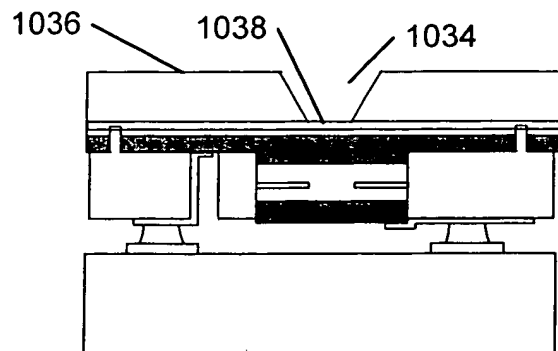
a)



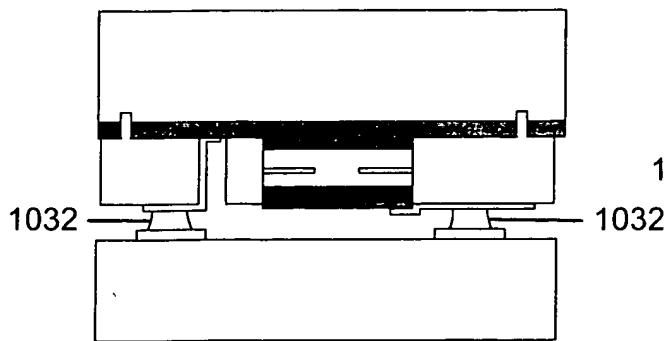
d)



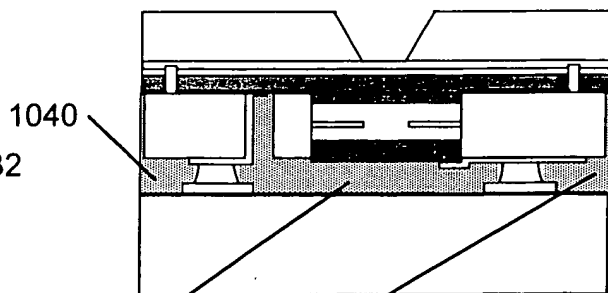
b)



e)



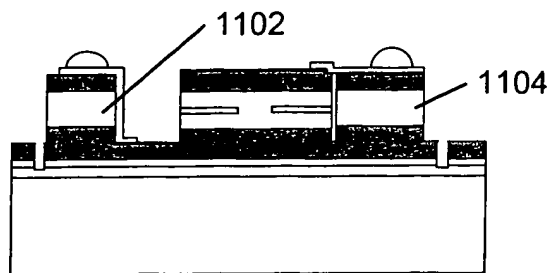
c)



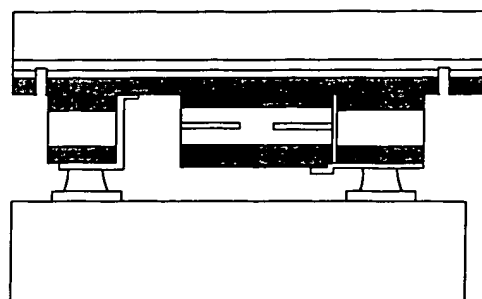
f)

FIG. 10

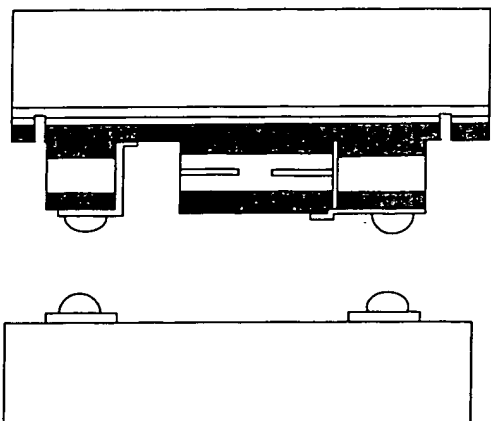




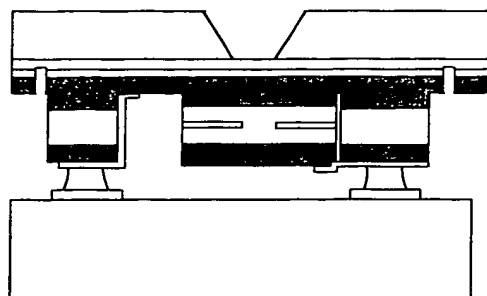
a)



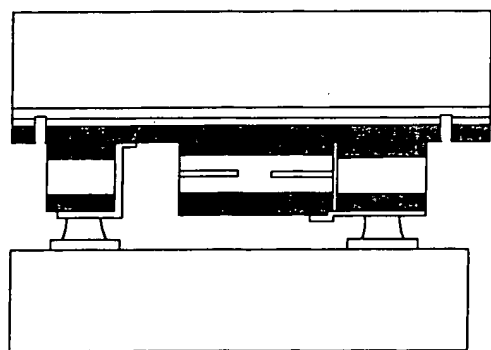
d)



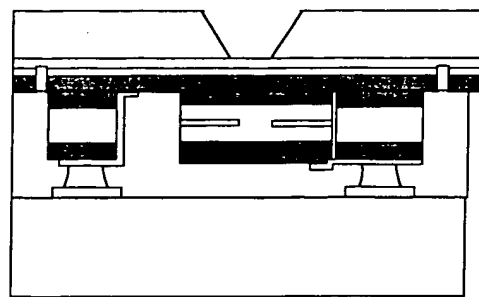
b)



e)



c)



f)

FIG. 11

FIG. 12

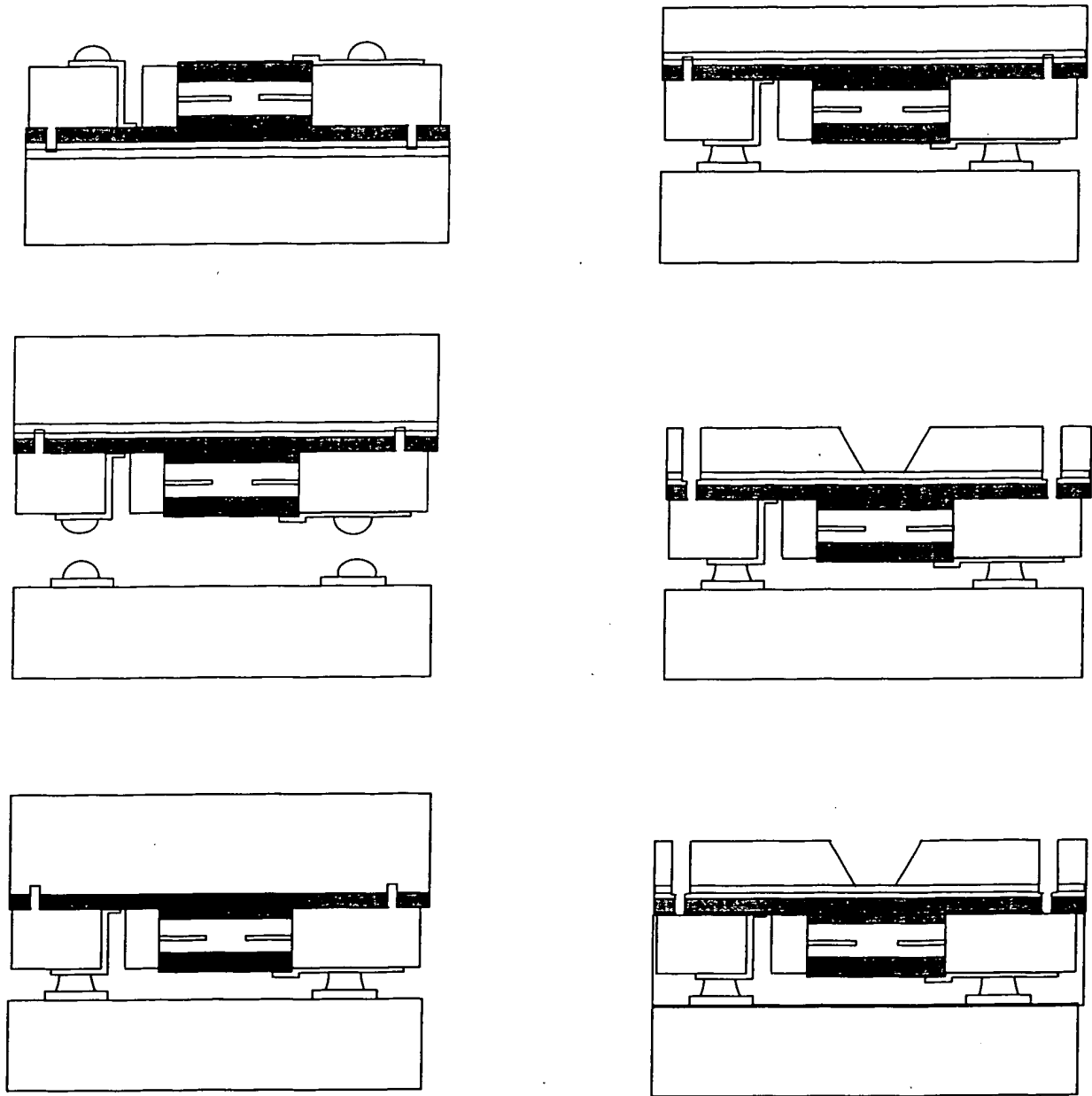
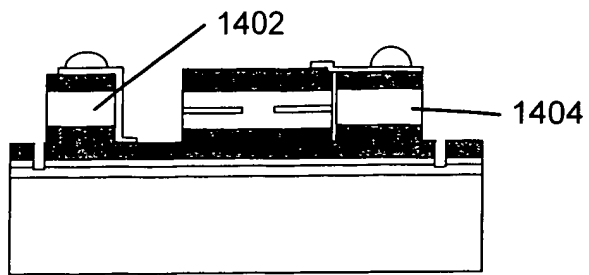
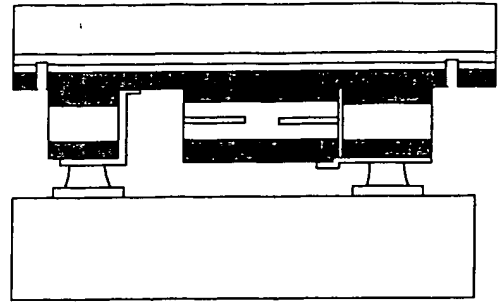


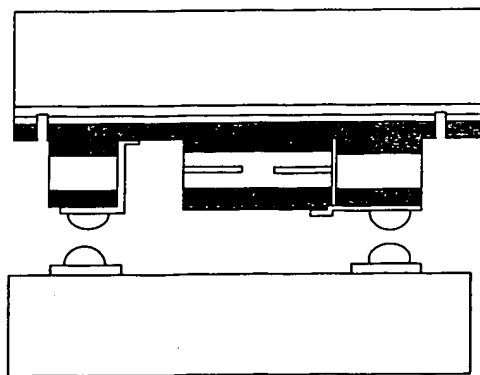
FIG. 12



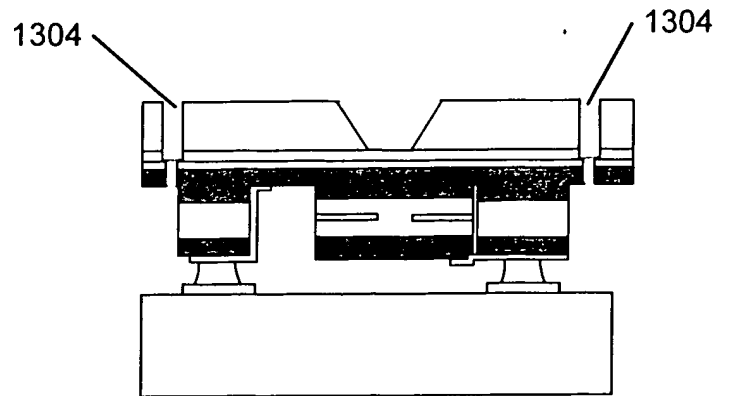
a)



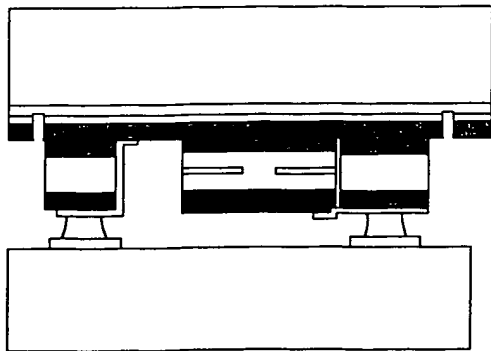
d)



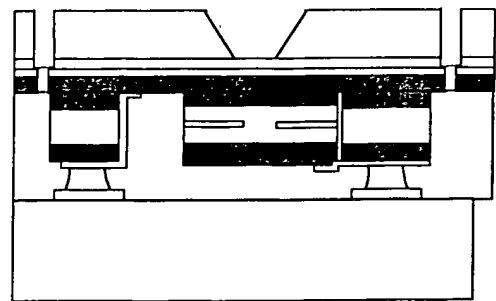
b)



e)



c)



f)

FIG. 14

FIG. 13

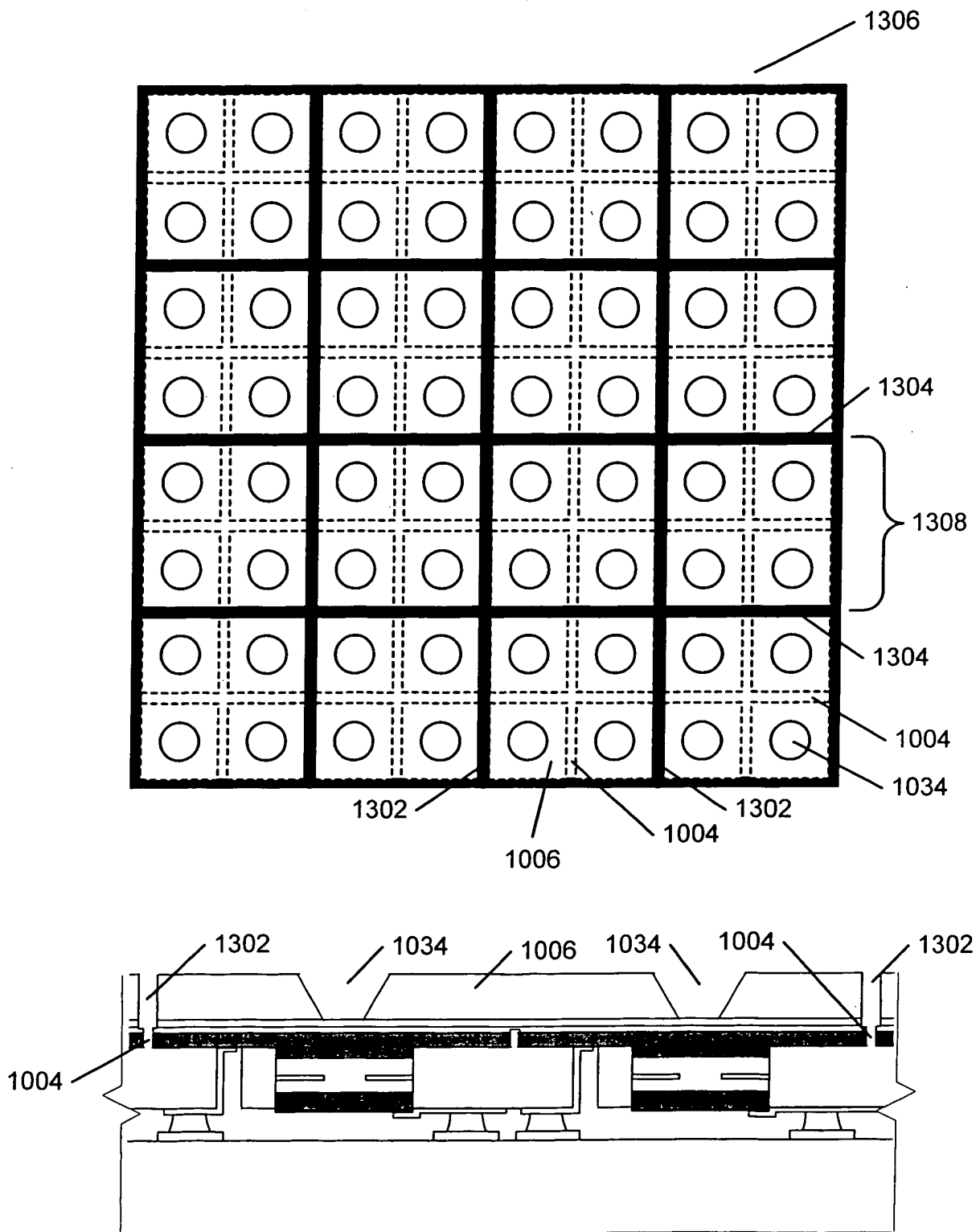
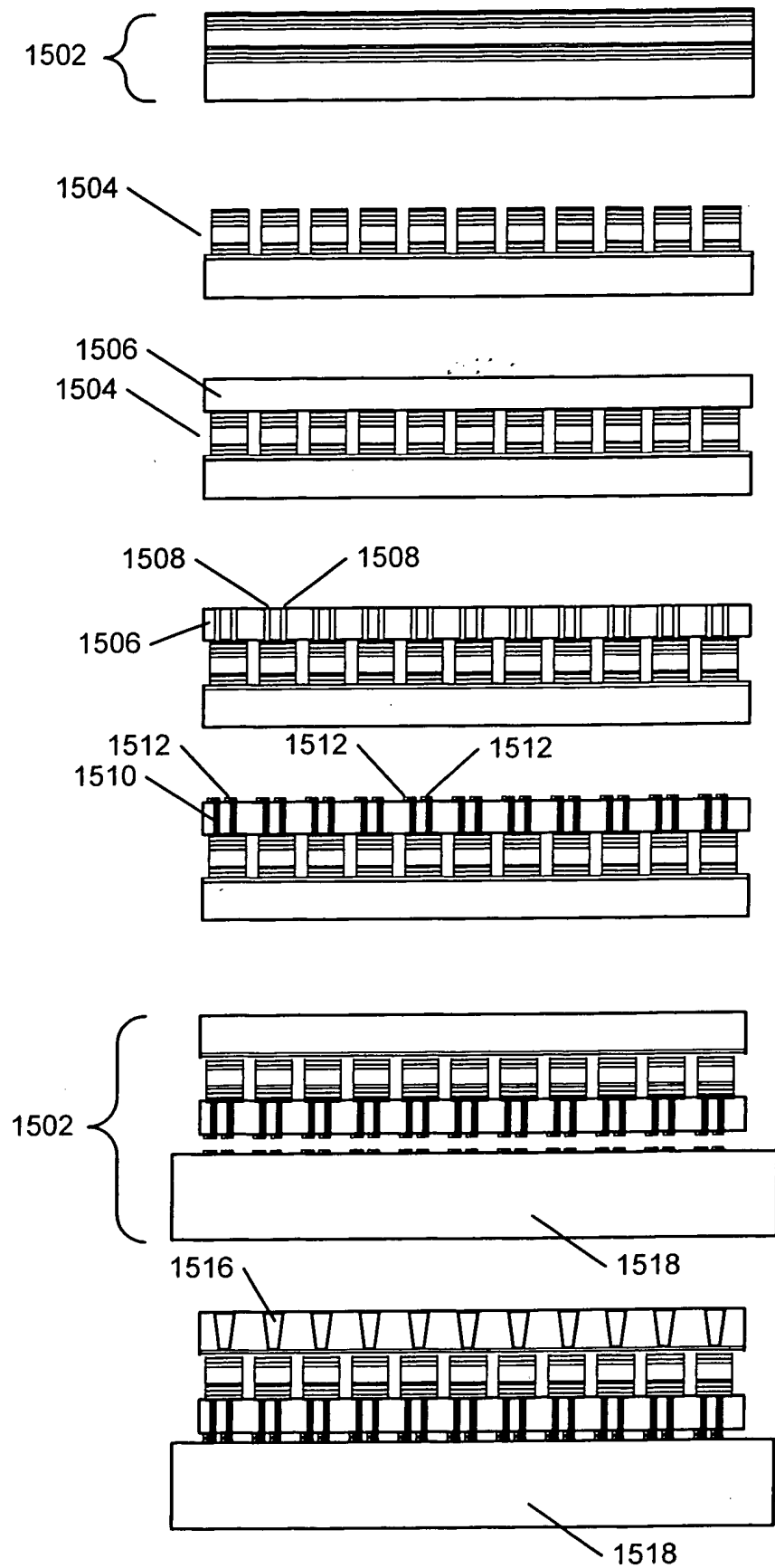


FIG. 13

FIG. 15



Optical wafers  
(e.g Laser and  
Detector wafers)

Process into  
individual devices

(Optional)  
Attach carrier

Thin substrate  
to appropriate  
thickness to  
facilitate etching

Etch vias (or drill  
holes) and pattern  
with insulator

Fill vias or holes  
with conductive  
material

Pattern wafer  
substrate to match  
pad locations on  
electronic chip

Attach optical  
chip to electronic  
chip using now  
matching pad  
locations

(Optional)  
Remove holder

(Optional) AR  
coat detectors

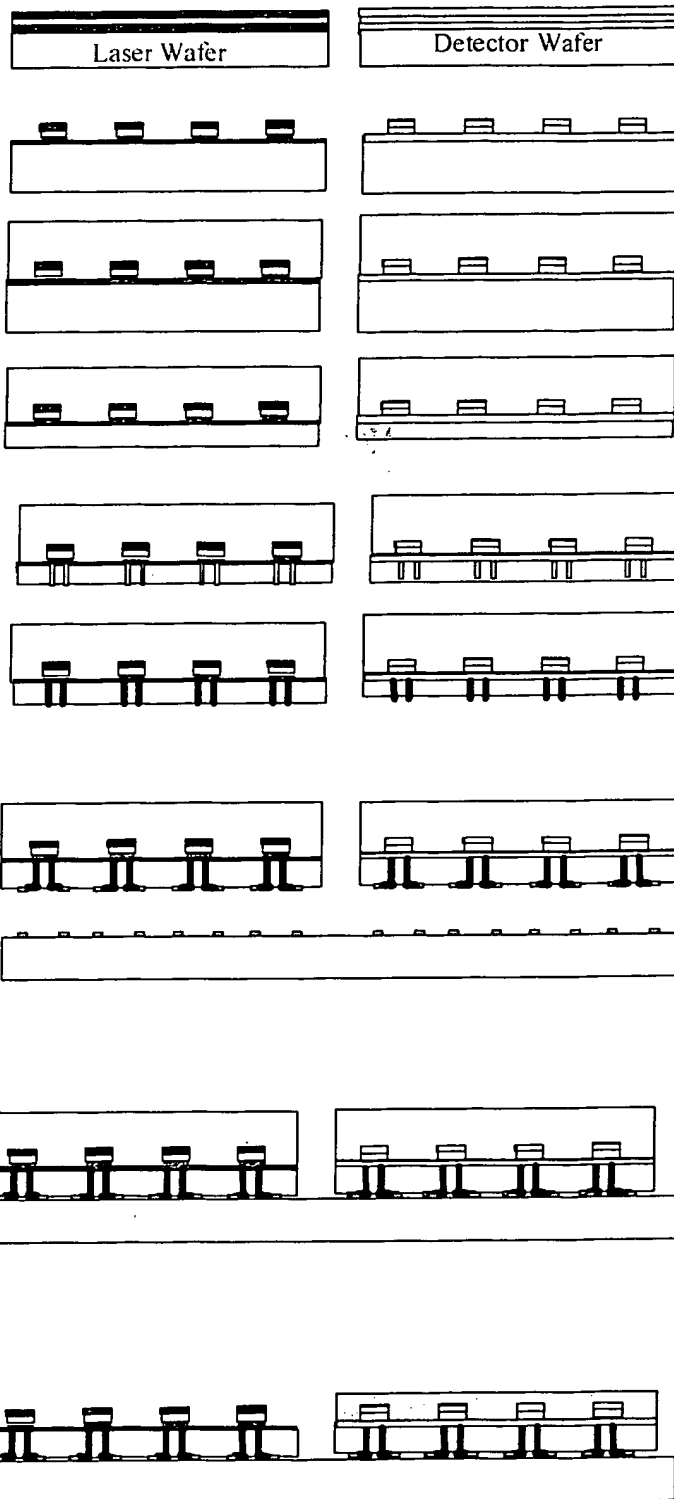
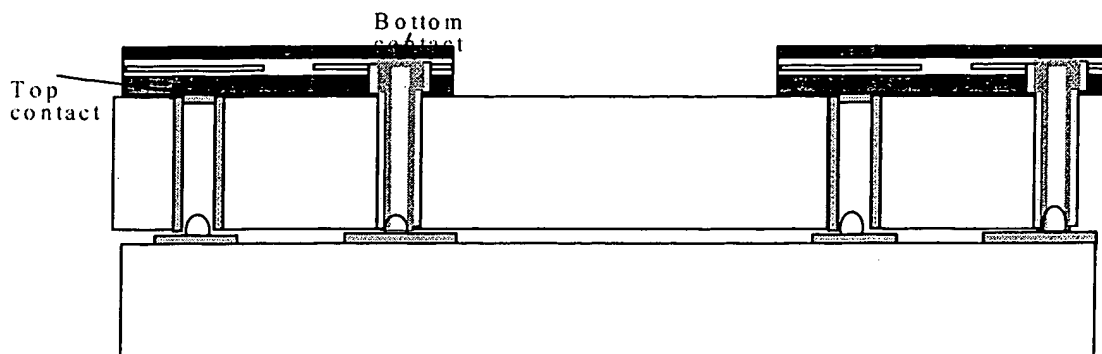
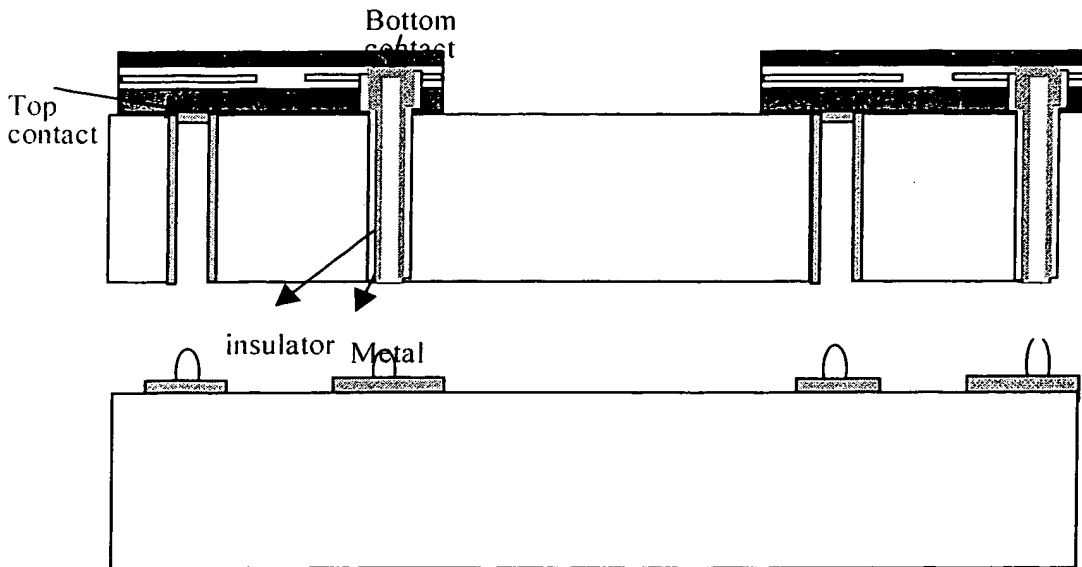
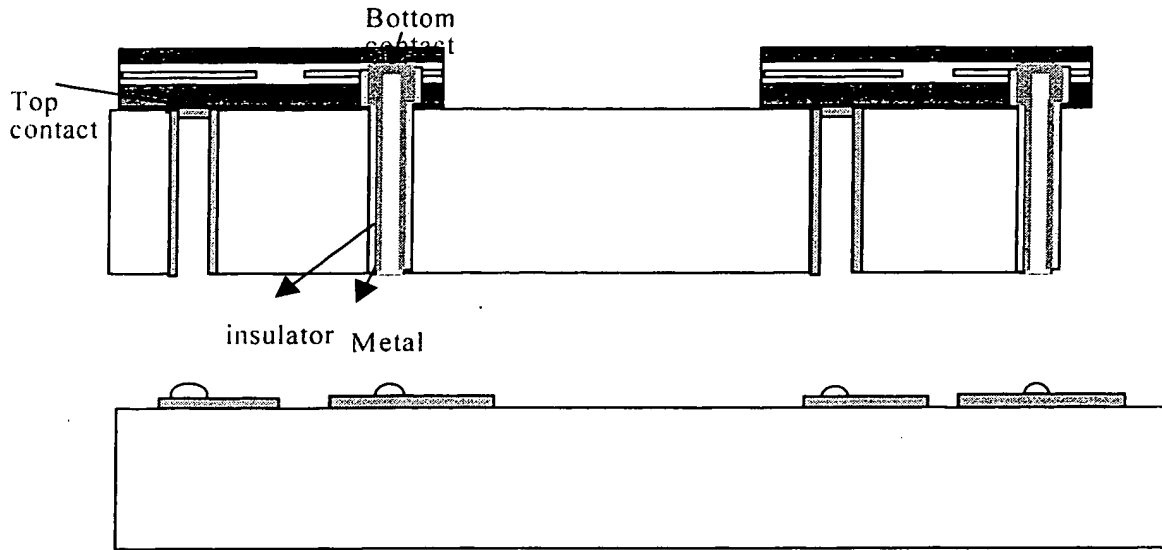


FIG. 16A

FIG. 16B



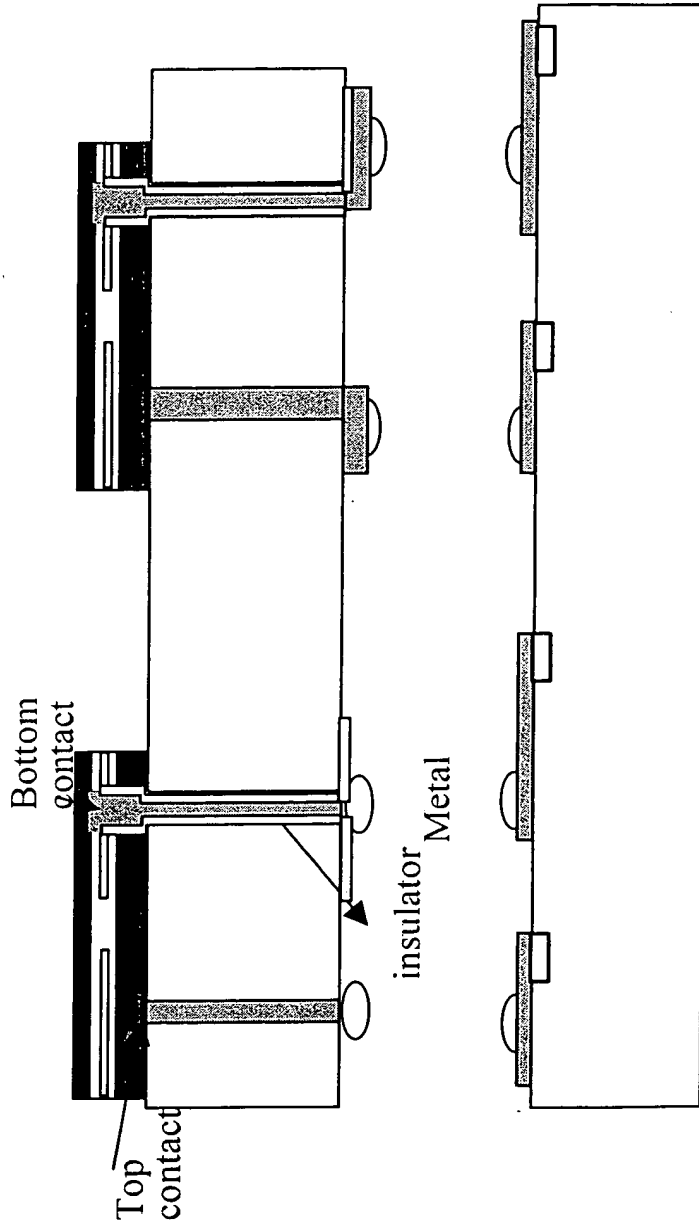


FIG. 16C



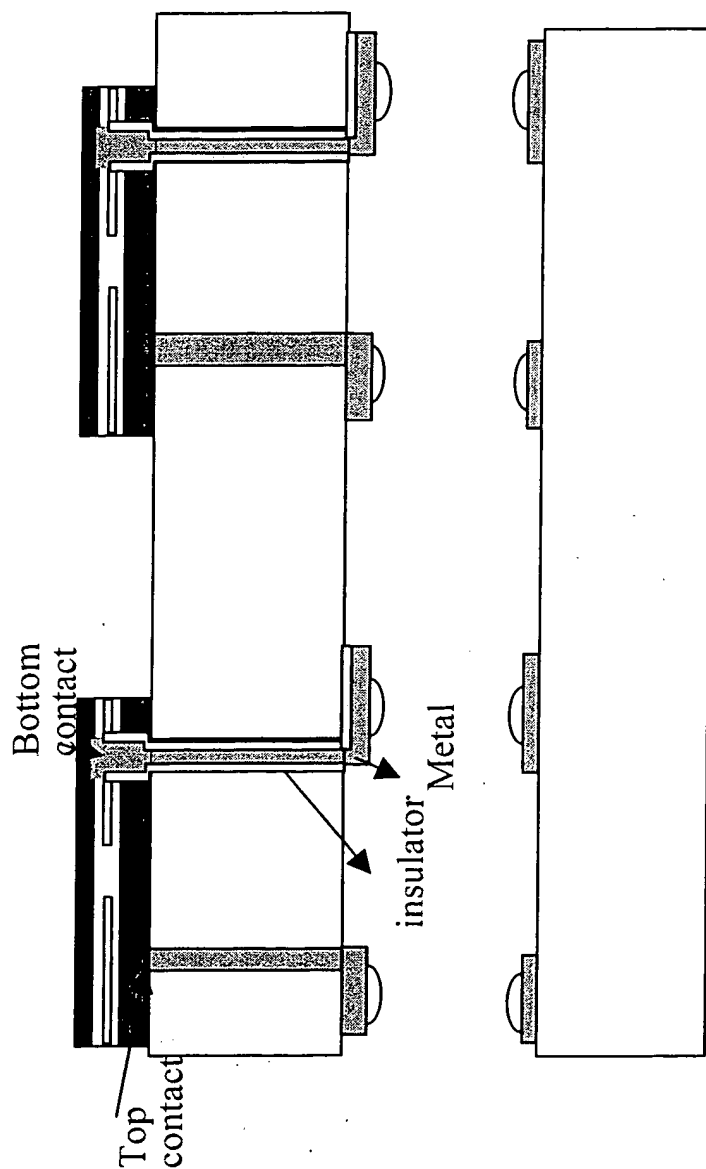


FIG. 16D



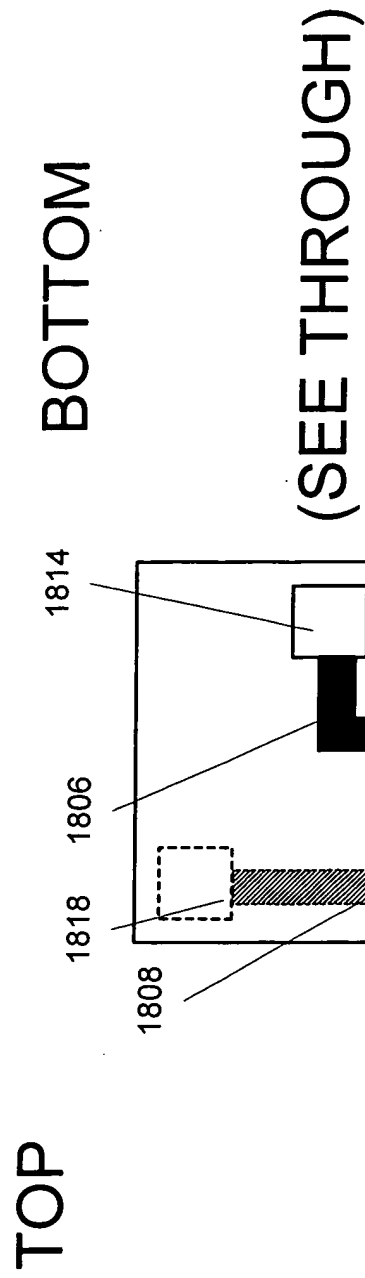
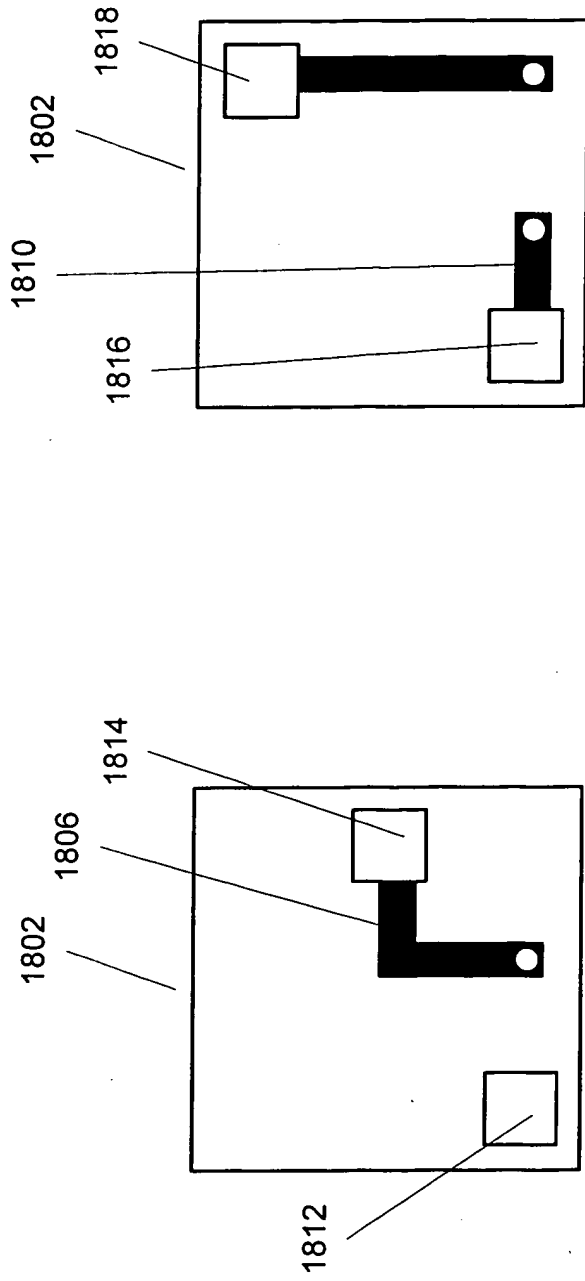


FIG. 18

# Optical wafers

(e.g Laser & Detector wafers)



Process into individual devices  
& AR coat detectors



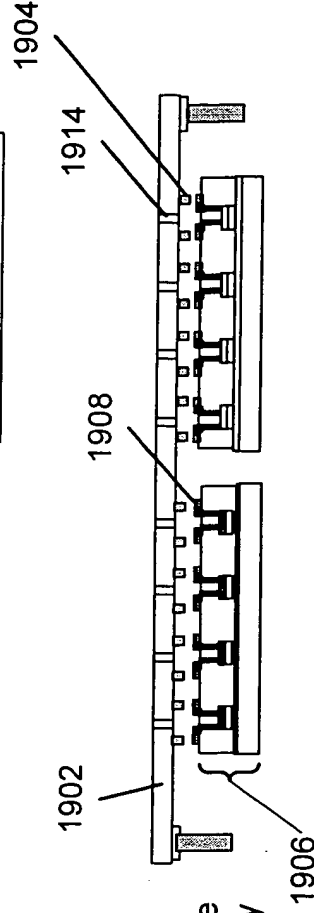
Cover devices with insulator and  
pattern vias through to device  
contact pads



Pattern optical device wafer  
to create traces to locations  
that will match mating  
contacts on adapter



Attach optical device chip  
to adapter via aligning  
pads created by patterning  
(NOTE: Holes in adapter can be  
created pre-post or concurrently  
with wafer patterning



Integrate adapter chip with  
electronic chip via standoffs,  
wires, etc.

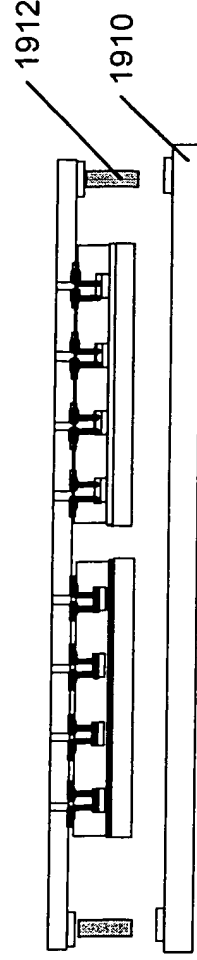


FIG. 19

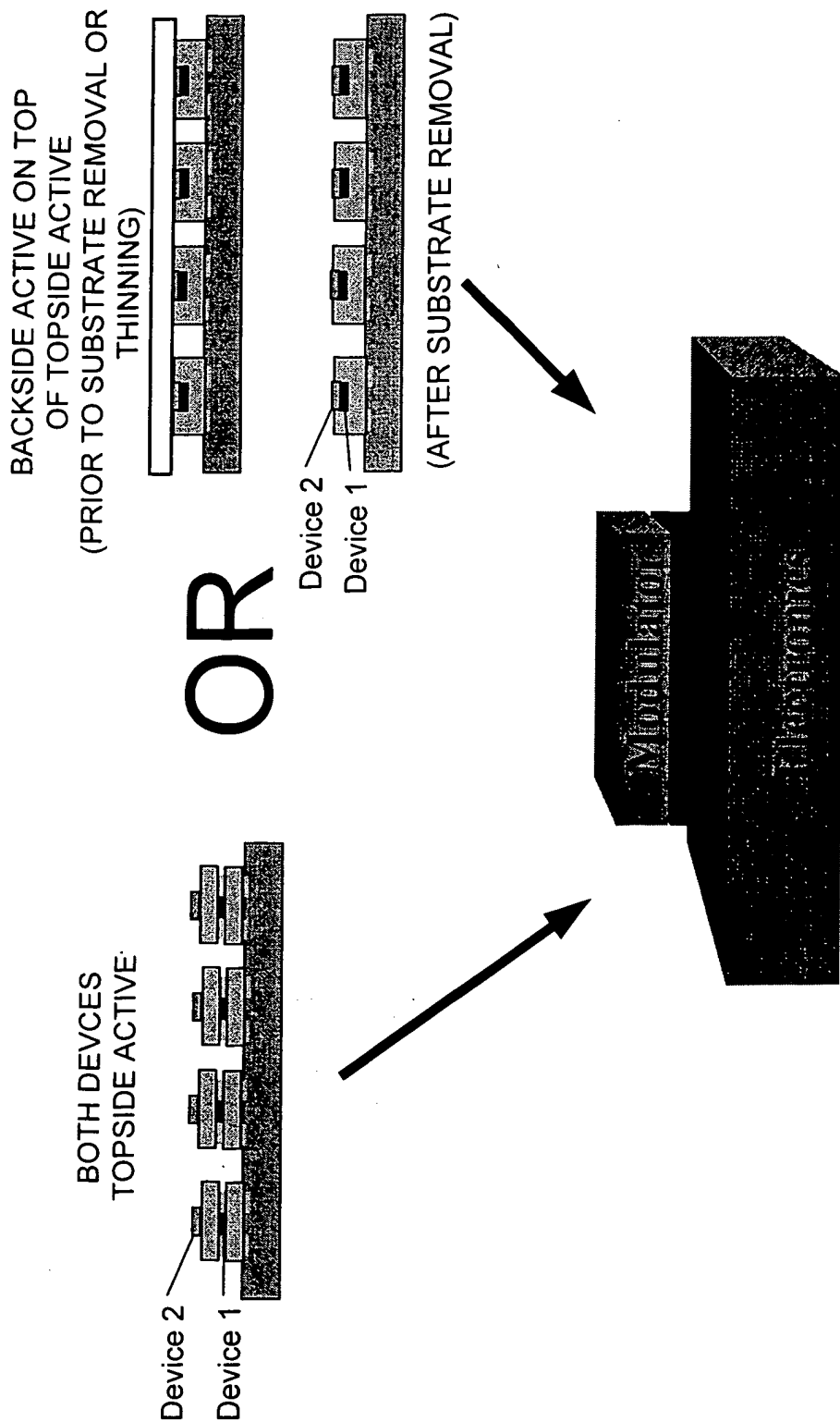


FIG. 20A

FIG. 20A

40 Gb/s = 20 GHz = 50ps  
Wavelength in free space =  $3 \times 10^{10} \text{ cm/s} \times 50^{12} \text{ s} = 1.5 \text{ cm}$   
1/8 wavelength in  $n=3 = 640 \text{ microns}$

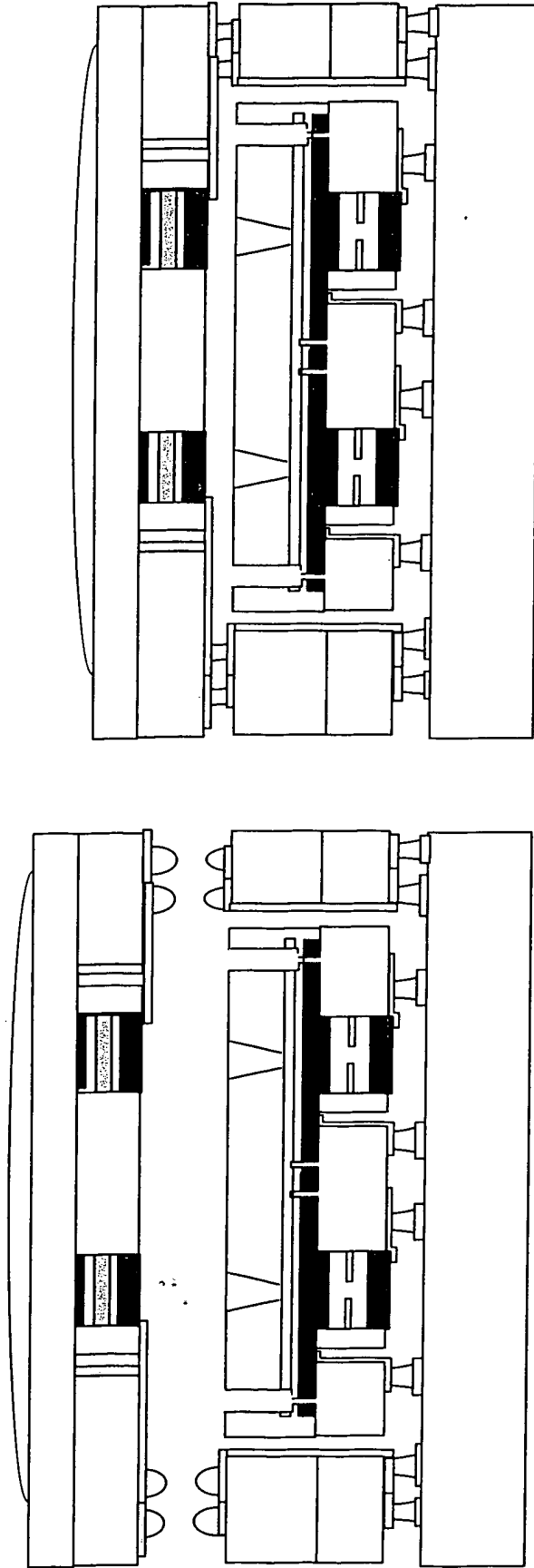


FIG. 20B

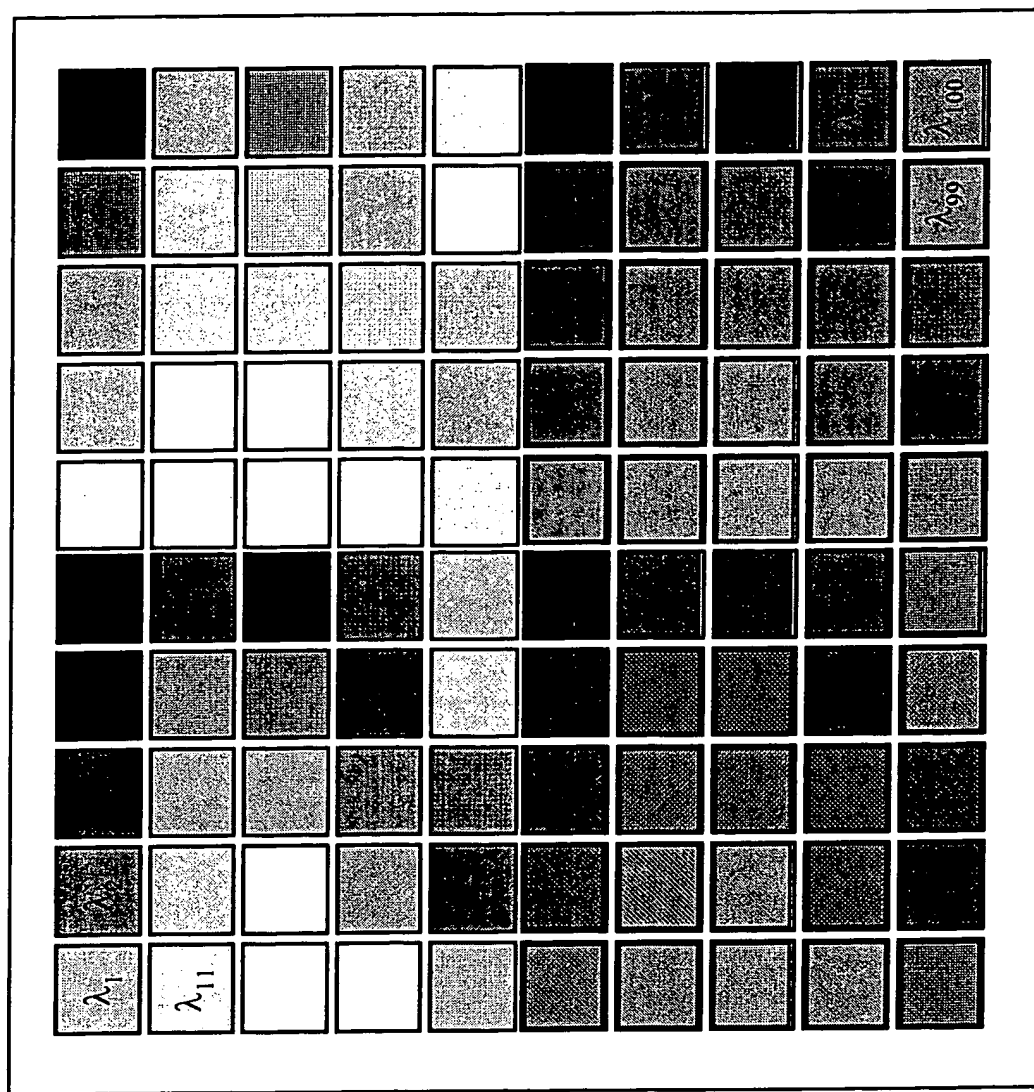


FIG. 21

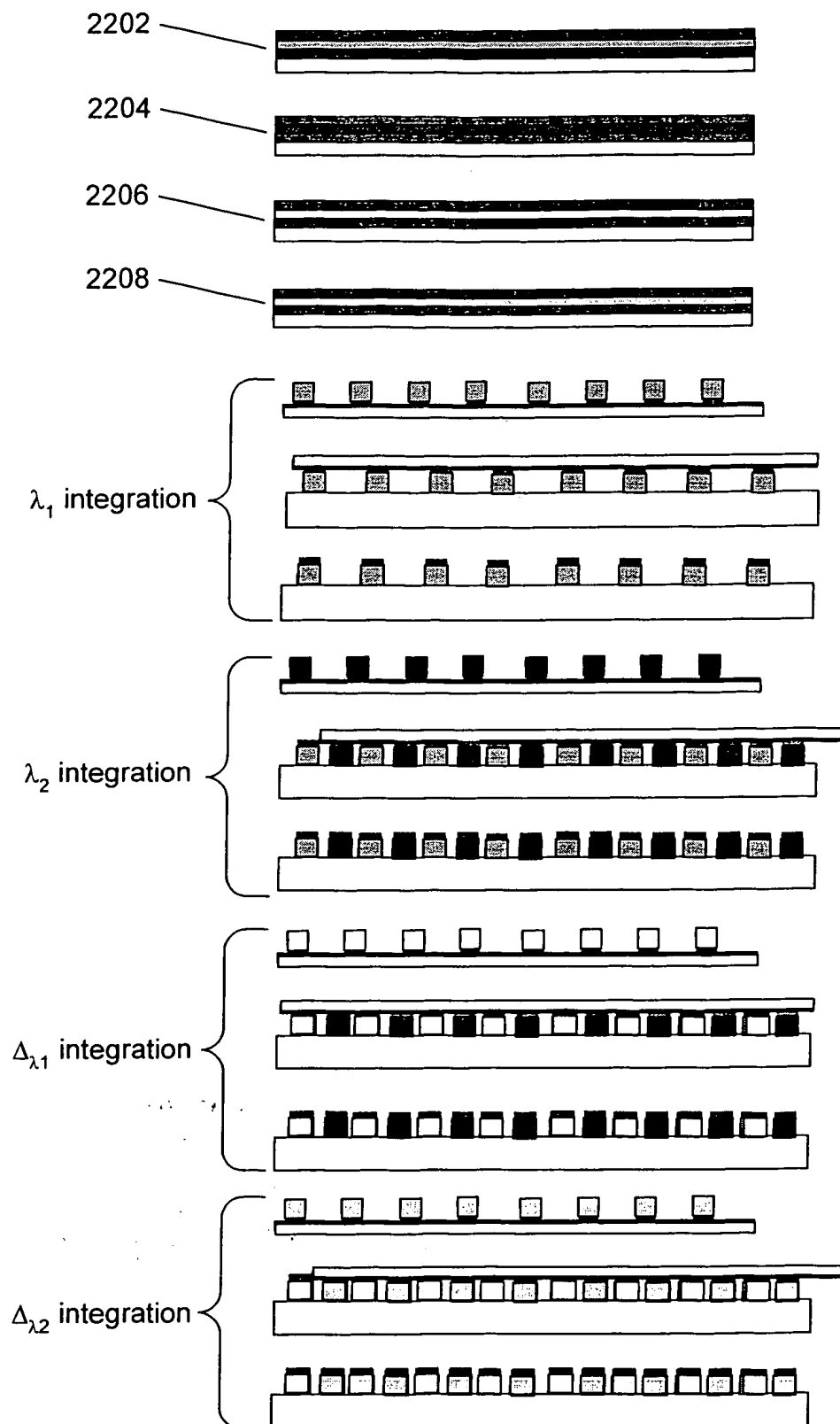
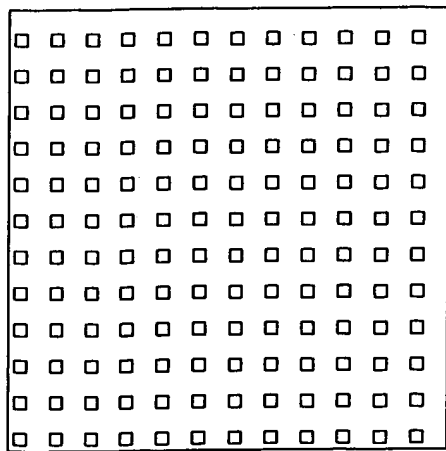
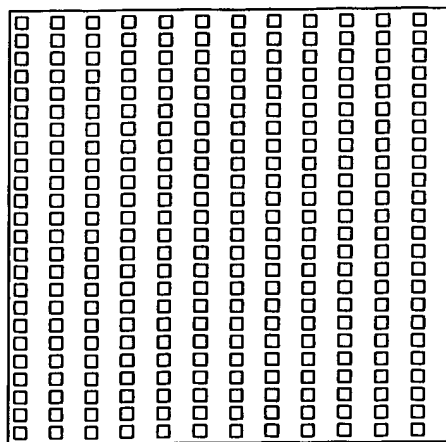


FIG. 22

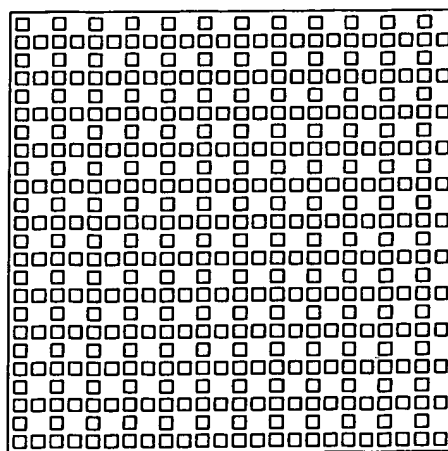




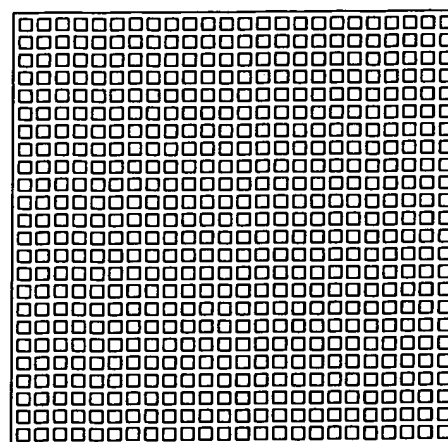
$\lambda_1$  integration



$\Delta\lambda_1$  integration



$\lambda_2$  integration



$\Delta\lambda_2$  integration

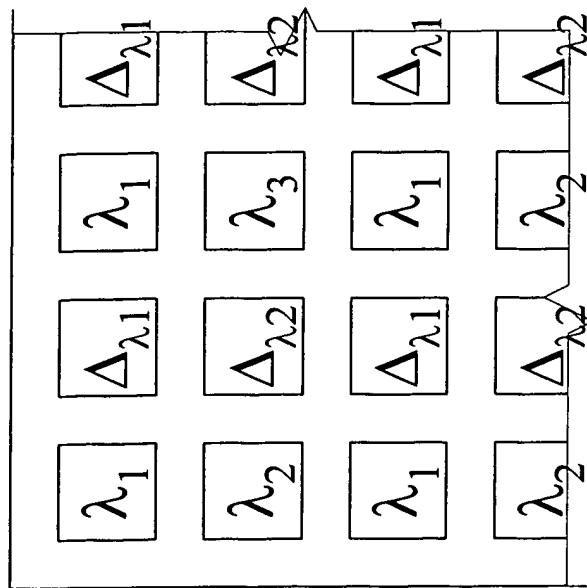


FIG. 23